IN THE TITLE OF THE INVENTION:

Please amend the title as it appears on the first page of the specification and in the U.S. Patent and Trademark Office records, as follows:

--~~METHOD~~ PROTECTION CIRCUIT FOR ~~PROTECTING~~ MOS COMPONENTS ~~FROM ANTENNA EFFECT AND THE APPARATUS THEREOF~~--

IN THE SPECIFICATION:

Please add the following paragraph before the heading beginning on page 1, line 7:

--This nonprovisional application claims priority under 35 U.S.C. § 119(a) on Patent Application No(s). 090105923 filed in Taiwan, R.O.C. on March 14, 2001, the entire contents of which are hereby incorporated by reference.--

Please amend the paragraph beginning on page 1, line 27, as follows:

--Fig.1 shows a conventional circuit design using a diode to reduce the antenna affect. In Fig.1, T1 is a MOS component in an integrated circuit (IC), the substrate (or bulk) B of the MOS is coupled to its own source, or to a fixed power rail (VDD or VSS).

The diode D1 has its anode coupled to the substrate of the IC. It is assumed that the conductive line L1 connected with the gate of the MOS component T1 has a very large surface area or periphery length. Due to the plasma characteristics, a large amount of charges is accumulated on the conductive line L1, causing the antenna affect (as the antenna Ana shown in Fig.1).--

Please amend the paragraph beginning on page 2, line 7, as follows:

--If the accumulated charges are negative charges, the diode D1 provides a discharge path to release the negative charges to the substrate sub1 of the IC, preventing damaging made to the gate oxide layer of the MOS component T1. However, when the accumulated charges are positive charges, no discharge path exists. The electric field across the gate oxide layer thus degrades the layer. Moreover, the large stray capacitance of the diode D1 compromises the operating rate of the IC circuit, resulting in slower operating speeds.--

Please amend the paragraph beginning on page 2, line 16, as follows:

--Fig.2 shows a conventional circuit design using a transmission gate to reduce the antenna effect. In Fig.2, the conductive line L2 connected to the gate of the MOS component T2 has very a large area or is very long. Due to the plasma distribution characteristics, large amounts of charges are accumulated on the conductive line L2, causing the antenna effect (as the antenna Ana shown in Fig.2). Herein, T2 is the MOS component of a IC circuit with its substrate B connected to the source or a fixed power rail (VDD or VSS).--

Please add the following paragraph before the heading beginning on page 4, line 22:

--Further scope of the applicability of the present invention will become apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.--

Please amend the paragraph beginning on page 5, line 1, as follows:

--Fig. 3 shows the embodiment of the present invention for reducing the antenna effect (as the antenna Ana shown in Fig. 3).--